

What is claimed is:

- 1 1. An add-compare-select apparatus for a Viterbi
2 decoder with a constraint length of K , comprising:
 - 3 a subtractor for calculating a path metric difference
4 by subtracting a path metric of state S_q at
5 instant $i-1$ from another path metric of state S_p
6 at instant $i-1$, where said path metrics are
7 represented by α bits of precision;
 - 8 a λ -bit multiplexer for selectively providing an output
9 between λ least significant bits of a branch
10 metric difference at instant i and the negative
11 thereof according to a select signal, where said
12 branch metric difference is represented by β bits
13 of precision and $\beta = \lambda + 1$;
 - 14 a λ -bit unsigned comparator for yielding a comparison
15 result by comparing the magnitude of λ least
16 significant bits of said α -bit path metric
17 difference and the magnitude of said λ -bit
18 multiplexer output;
 - 19 a first combinational-logic circuit for logically
20 operating δ most significant bits of said α -bit
21 path metric difference and a sign bit of said
22 branch metric difference at instant i to
23 predetermine whether the magnitude of said α -bit
24 path metric difference is greater than that of
25 said branch metric difference, setting a decision
26 bit of state S_u at instant i based on a
27 predetermination made therein if said
28 predetermination is met, and setting said

29 decision bit of state S_u at instant i to be
30 consistent with said comparison result if said
31 predetermination is not met, where $\delta = \alpha - \lambda$;
32 a second combinational-logic circuit for logically
33 operating δ most significant bits of said α -bit
34 path metric difference and said sign bit of said
35 branch metric difference at instant i to
36 predetermine whether the magnitude of said α -bit
37 path metric difference is greater than that of
38 the negative of said branch metric difference,
39 setting a decision bit of state S_v at instant i
40 based on another predetermination made therein if
41 said another predetermination is met, and setting
42 said decision bit of state S_v at instant i to be
43 consistent with said comparison result if said
44 another predetermination is not met;
45 a first adding means, according to said decision bit of
46 state S_u at instant i , for calculating a new path
47 metric for state S_u at instant i by selectively
48 adding said path metric of state S_q at instant $i-1$
49 and a branch metric of a transition from state S_q
50 to state S_u at instant i or adding said another
51 path metric of state S_p at instant $i-1$ and another
52 branch metric of a second transition from state S_p
53 to state S_u at instant i , where said branch
54 metrics are represented by λ bits of precision;
55 and
56 a second adding means, according to said decision bit
57 of state S_v at instant i , for calculating another
58 new path metric for state S_v at instant i by

59 selectively adding said path metric of state S_q at
60 instant $i-1$ and said another branch metric of
61 said second transition from state S_p to state S_u
62 at instant i or adding said another path metric of
63 state S_p at instant $i-1$ and said branch metric of
64 said transition from state S_q to state S_u at
65 instant i ;
66 wherein said branch metric difference is pre-calculated
67 by subtracting said another branch metric of said
68 second transition from state S_p to state S_u at
69 instant i from said branch metric of said
70 transition from state S_q to state S_u at instant i ;
71 wherein states S_p and S_q at instant $i-1$ and states S_u
72 and S_v at instant i are organized in a butterfly
73 trellis structure, and subscripts p , q , u and v
74 are given by:

$$\begin{aligned} p &= 0, 1, 2, \dots, 2^{K-2} - 1 \\ q &= 2^{K-2} + p \\ u &= 2p \\ v &= 2p + 1. \end{aligned}$$

1 2. The apparatus as recited in claim 1 wherein said
2 first combinational-logic circuit is capable of setting said
3 select signal depending on whether said branch metric
4 difference at instant i and said path metric difference at
5 instant $i-1$ both have the same sign.

1 3. The apparatus as recited in claim 1 wherein said
2 second combinational-logic circuit is capable of setting
3 said select signal depending on whether said branch metric

4 difference at instant i and said path metric difference at
5 instant $i-1$ both have the same sign.

1 4. The apparatus as recited in claim 1 further
2 comprising means for predetermining a local winner state
3 between states S_u and S_v at instant i based on said decision
4 bits of states S_u and S_v at instant i , and the sign of said
5 path metric difference at instant $i-1$ or the sign of said
6 branch metric difference at instant i , whereby a saving of
7 half the output number of said new path metrics at instant i
8 is achieved.

1 5. An apparatus for branch metric computation and add-
2 compare-select operation in a rate $1/n$ Viterbi decoder with
3 a constraint length of K , comprising:

4 a branch metric generator receiving a data symbol
5 including n decision metrics in Q -bit
6 representation, for calculating a plurality of
7 branch metrics each of which is a measure between
8 said currently received data symbol and a
9 corresponding branch label, and further pre-
10 calculating a branch metric difference by
11 subtracting a first branch metric of a transition
12 from state S_p to state S_u at instant i from a
13 second branch metric of another transition from
14 state S_q to state S_u at instant i ; and
15 an add-compare-select unit receiving said first branch
16 metric of said transition from state S_p to state
17 S_u , said second branch metric of said another
18 transition from state S_q to state S_u and said
19 branch metric difference at instant i from said

20 branch metric generator and calculating a path
21 metric difference between a path metric of state
22 S_p at instant $i-1$ and another path metric of state
23 S_q at instant $i-1$, for respectively setting
24 decision bits of states S_u and S_v at instant i
25 based on said branch metric difference at instant
26 i and said path metric difference, comprising:
27 a first adding means, according to said decision
28 bit of state S_u at instant i , for calculating
29 a new path metric for state S_u at instant i
30 by selectively adding said another path
31 metric of state S_q at instant $i-1$ and said
32 second branch metric of said another
33 transition from state S_q to state S_u at
34 instant i or adding said path metric of
35 state S_p at instant $i-1$ and said first
36 branch metric of said transition from state
37 S_p to state S_u at instant i ;
38 a second adding means, according to said decision
39 bit of state S_v at instant i , for calculating
40 another new path metric for state S_v at
41 instant i by selectively adding said another
42 path metric of state S_q at instant $i-1$ and
43 said first branch metric of said transition
44 from state S_p to state S_u at instant i or
45 adding said path metric of state S_p at
46 instant $i-1$ and said second branch metric of
47 said another transition from state S_q to
48 state S_u at instant i ; and

49 means for selectively outputting one of said new
50 path metrics, which is a survivor path
51 metric of a local winner state, by
52 predetermining said local winner state
53 between states S_u and S_v at instant i based on
54 said decision bits of states S_u and S_v at
55 instant i , and the sign of said path metric
56 difference at instant $i-1$ or the sign of
57 said branch metric difference at instant i ;
58 wherein states S_p and S_q at instant $i-1$ and states S_u
59 and S_v at instant i are organized in a butterfly
60 trellis structure, and subscripts p , q , u and v
61 are given by:

$$\begin{aligned} p &= 0, 1, 2, \dots, 2^{K-2} - 1 \\ q &= 2^{K-2} + p \\ u &= 2p \\ v &= 2p + 1. \end{aligned}$$

1 6. The apparatus as recited in claim 5 wherein said
2 add-compare-select unit further comprises:
3 a subtractor for calculating said path metric
4 difference by subtracting said another path
5 metric of state S_q at instant $i-1$ from said path
6 metric of state S_p at instant $i-1$, where said path
7 metrics are represented by α bits of precision,
8 respectively;
9 a λ -bit multiplexer for selectively providing an output
10 between λ least significant bits of said branch
11 metric difference at instant i and the negative
12 thereof according to a select signal, where said

13 branch metric difference is represented by β bits
14 of precision and $\beta = \lambda + 1$;
15 a λ -bit unsigned comparator for yielding a comparison
16 result by comparing the magnitude of λ least
17 significant bits of said α -bit path metric
18 difference and the magnitude of said λ -bit
19 multiplexer output;
20 a first combinational-logic circuit for logically
21 operating δ most significant bits of said α -bit
22 path metric difference and a sign bit of said
23 branch metric difference at instant i to
24 predetermine whether the magnitude of said α -bit
25 path metric difference is greater than that of
26 said branch metric difference, setting said
27 decision bit of state S_u at instant i based on a
28 predetermination made therein if said
29 predetermination is met, and setting said
30 decision bit of state S_u at instant i to be
31 consistent with said comparison result if said
32 predetermination is not met, where $\delta = \alpha - \lambda$; and
33 a second combinational-logic circuit for logically
34 operating δ most significant bits of said α -bit
35 path metric difference and said sign bit of said
36 branch metric difference at instant i to
37 predetermine whether the magnitude of said α -bit
38 path metric difference is greater than that of
39 the negative of said branch metric difference,
40 setting said decision bit of state S_v at instant i
41 based on another predetermination made therein if
42 said another predetermination is met, and setting

43 said decision bit of state S_i at instant i to be
44 consistent with said comparison result if said
45 another predetermination is not met.

1 7. The apparatus as recited in claim 6 wherein said
2 first combinational-logic circuit is capable of setting said
3 select signal depending on whether said branch metric
4 difference at instant i and said path metric difference at
5 instant $i-1$ both have the same sign.

1 8. The apparatus as recited in claim 6 wherein said
2 second combinational-logic circuit is capable of setting
3 said select signal depending on whether said branch metric
4 difference at instant i and said path metric difference at
5 instant $i-1$ both have the same sign.

1 9. The apparatus as recited in claim 6 wherein said
2 branch metrics are represented by λ bits of precision, in
3 which λ is given by:

$$4 \quad \lambda = Q + n - 1$$

1 10. The apparatus as recited in claim 9 wherein the
2 number of bits of precision representing said path metrics,
3 α , is given by:

$$4 \quad \alpha = 1 + \lceil \log_2(n \cdot K(2^Q - 1)) \rceil$$

5 where $\lceil \cdot \rceil$ denotes a ceiling function.

1 11. The apparatus as recited in claim 5 further
2 comprising:

3 a dummy insertion unit for performing a dummy insertion
4 procedure inverse to a bit-stealing procedure in

5 a transmitter according to a puncturing pattern
6 and outputting a dummy insertion flag to indicate
7 a position at which a dummy value is inserted
8 into said decision metrics.

1 12. The apparatus as recited in claim 11 wherein said
2 branch metric generator ignores said inserted dummy value in
3 response to said dummy insertion flag when calculating said
4 branch metrics for said n decision metrics including said
5 inserted dummy value.

1 13. A rate $1/n$ Viterbi decoder with a constraint length
2 of K , comprising:

3 a dummy insertion unit for performing a dummy insertion
4 procedure, which is inverse to a bit-stealing
5 procedure in a transmitter, on a sequence of
6 decision metrics in Q -bit representation
7 according to a puncturing pattern and outputting
8 a dummy insertion flag to indicate a position at
9 which a dummy value is inserted into said
10 decision metrics;

11 a branch metric generator receiving n number of said
12 decision metrics including said dummy value to
13 group into a data symbol, for calculating a
14 plurality of branch metrics each of which is a
15 measure between said data symbol and a
16 corresponding branch label, and further pre-
17 calculating a branch metric difference for a p th
18 sub-group of states including states S_p , S_q , S_u and
19 S_v by subtracting a first branch metric of a
20 transition from state S_p to state S_u at instant i

21 from a second branch metric of another transition
22 from state S_q to state S_u at instant i , wherein
23 said dummy value is ignored in response to said
24 dummy insertion flag when said branch metrics are
25 calculated for said data symbol;
26 *P* add-compare-select units, in which a p th add-compare-
27 select unit receives said first branch metric of
28 said transition from state S_p to state S_u , said
29 second branch metric of said another transition
30 from state S_q to state S_u and said branch metric
31 difference for the p th sub-group of states at
32 instant i from said branch metric generator and
33 calculates a path metric difference between a
34 path metric of state S_p at instant $i-1$ and another
35 path metric of state S_q at instant $i-1$, for
36 setting a pair of decision bits for states S_u and
37 S_v at instant i based on said branch metric
38 difference at instant i and said path metric
39 difference, respectively generating new path
40 metrics for states S_u and S_v at instant i , further
41 predetermining a local winner state between
42 states S_u and S_v at instant i based on said
43 decision bits of states S_u and S_v at instant i , and
44 the sign of said branch metric difference at
45 instant i or the sign of said path metric
46 difference, and providing one of said new path
47 metrics as output, which is a survivor path
48 metric of said local winner state at instant i , to
49 achieve a saving of half the output number of
50 said new path metrics; and

51 a survivor memory unit receiving said P survivor path
52 metrics of said P local winner states and said P
53 pairs of decision bits at instant i from said P
54 add-compare-select units, for storing survivor
55 path sequences and yielding a decoded bit
56 sequence;

57 wherein states S_p and S_q at instant $i-1$ and states S_u
58 and S_v at instant i are organized in a butterfly
59 trellis structure, and subscripts p , q , u and v
60 are given by:

61
$$p = 0, 1, 2, \dots, P-1$$

62
$$q = P + p$$

63
$$u = 2p$$

64
$$v = 2p + 1$$

65 where $P = 2^{K-2}$.

1 14. The Viterbi decoder as recited in claim 13 wherein
2 the p th add-compare-select unit comprises:

3 a subtractor for calculating said path metric
4 difference by subtracting said another path
5 metric of state S_q at instant $i-1$ from said path
6 metric of state S_p at instant $i-1$, where said path
7 metrics are represented by α bits of precision,
8 respectively;

9 a λ -bit multiplexer for selectively providing an output
10 between λ least significant bits of said branch
11 metric difference at instant i and the negative
12 thereof according to a select signal, where said
13 branch metric difference is represented by β bits
14 of precision and $\beta = \lambda + 1$;

15 a λ -bit unsigned comparator for yielding a comparison
16 result by comparing the magnitude of λ least
17 significant bits of said α -bit path metric
18 difference and the magnitude of said λ -bit
19 multiplexer output;
20 a first combinational-logic circuit for logically
21 operating δ most significant bits of said α -bit
22 path metric difference and a sign bit of said
23 branch metric difference at instant i to
24 predetermine whether the magnitude of said α -bit
25 path metric difference is greater than that of
26 said branch metric difference, setting said
27 decision bit of state S_u at instant i based on a
28 predetermination made therein if said
29 predetermination is met, and setting said
30 decision bit of state S_u at instant i to be
31 consistent with said comparison result if said
32 predetermination is not met, where $\delta = \alpha - \lambda$; and
33 a second combinational-logic circuit for logically
34 operating δ most significant bits of said α -bit
35 path metric difference and said sign bit of said
36 branch metric difference at instant i to
37 predetermine whether the magnitude of said α -bit
38 path metric difference is greater than that of
39 the negative of said branch metric difference,
40 setting said decision bit of state S_v at instant i
41 based on another predetermination made therein if
42 said another predetermination is met, and setting
43 said decision bit of state S_v at instant i to be

44 consistent with said comparison result if said
45 another predetermination is not met.

1 15. The Viterbi decoder as recited in claim 14 wherein
2 the p th add-compare-select unit further comprises:

3 a first adding means, according to said decision bit of
4 state S_u at instant i , for calculating said new
5 path metric of state S_u at instant i by
6 selectively adding said another path metric of
7 state S_q at instant $i-1$ and said second branch
8 metric of said another transition from state S_q to
9 state S_u at instant i or adding said path metric
10 of state S_p at instant $i-1$ and said first branch
11 metric of said transition from state S_p to state
12 S_u at instant i ; and

13 a second adding means, according to said decision bit
14 of state S_v at instant i , for calculating said new
15 path metric of state S_v at instant i by
16 selectively adding said another path metric of
17 state S_q at instant $i-1$ and said first branch
18 metric of said transition from state S_p to state
19 S_u at instant i or adding said path metric of
20 state S_p at instant $i-1$ and said second branch
21 metric of said another transition from state S_q to
22 state S_u at instant i .

1 16. The Viterbi decoder as recited in claim 14 wherein
2 said first combinational-logic circuit is capable of setting
3 said select signal depending on whether said branch metric
4 difference at instant i and said path metric difference at
5 instant $i-1$ both have the same sign.

Client's ref.: P47US

Our ref.: 0751-10281US/final/M.F.Lin/Kevin

1 17. The Viterbi decoder as recited in claim 14 wherein
2 said second combinational-logic circuit is capable of
3 setting said select signal depending on whether said branch
4 metric difference at instant i and said path metric
5 difference at instant $i-1$ both have the same sign.

1 18. The Viterbi decoder as recited in claim 14 wherein
2 said branch metrics are represented by λ bits of precision,
3 in which λ is given by:

4
$$\lambda = Q + n - 1$$

1 19. The Viterbi decoder as recited in claim 14 wherein
2 the number of bits of precision representing said path
3 metrics, α , is given by:

4
$$\alpha = 1 + \lceil \log_2(n \cdot K(2^Q - 1)) \rceil$$

5 where $\lceil \cdot \rceil$ denotes a ceiling function.

1 20. The Viterbi decoder as recited in claim 13 wherein
2 said decision metrics are hard-decision data if quantized to
3 one bit of precision.